CLAIMS

1. A charge pump, comprising:

a first capacitor having first and second terminals, the first terminal being coupled to a pumped node;

a second capacitor having first and second terminals, the first terminal being coupled to the pumped node;

a charging circuit coupled to the pumped node, the charging circuit being operable to charge the first and second capacitors through the pumped node responsive to a charge enable signal;

a first pumping circuit having an output signal, the first pumping circuit transitioning the output signal from a first logic level to a second logic level responsive to a predetermined transition of a first control signal;

a second pumping circuit having an output signal, the second pumping circuit transitioning the output signal from a third logic level to a fourth logic level responsive to a predetermined transition of a second control signal;

a first isolation circuit coupled between the output of the first pumping circuit and the second terminal of the first capacitor, the first isolation circuit isolating the first pumping circuit from the second terminal of the first capacitor responsive to a first logic level of an isolation signal and coupling the output of the first pumping circuit to the second terminal of the first capacitor responsive to a second logic level of the isolation signal; and

an output circuit coupled to the pumped node, the output circuit being operable to couple the pumped node to an output terminal responsive to an output enable signal; and

a control circuit operable to generate the charge enable signal, the first and second control signals, the first isolation signal, and the output enable signal.

2. The charge pump of claim 1, wherein the control circuit is operable to generate the charge enable signal, the first, second, third and fourth control signals, the first and second isolation signals, and the output enable signal in the order of:

the charge enable signal;

the predetermined transition of the first control signal;

the first isolation signal;

the predetermined transition of the second control signal; and

the output enable signal.

3. The charge pump of claim 1, further comprising:

a second isolation circuit coupled between the output of the second pumping circuit and the second terminal of the second capacitor, the second isolation circuit isolating the second pumping circuit from the second terminal of the second capacitor responsive to a first logic level of a second isolation signal and coupling the output of the second pumping circuit to the second terminal of the second capacitor responsive to a second logic level of the second isolation signal; and

wherein the control circuit is further operable to generate the second isolation signal.

4. The charge pump of claim 1 wherein the first isolation circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to the second terminal of the first capacitor and a second source-drain terminal coupled to receive the output signal of the first pumping circuit;

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal responsive to a transition of the isolation signal from the first logic level to the second logic level to a magnitude sufficient to allow the transistor to pass the second logic level of the output from the first pumping circuit to the second terminal of the first capacitor.

5. The charge pump of claim 1 wherein the charging circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to a charging voltage and a second source-drain terminal coupled to the pumped node; and

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal responsive to a transition of the charge enable signal to a magnitude sufficient to allow the charging voltage to be coupled through the transistor to the pumped node.

6. The charge pump of claim 1 wherein the output circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to the pumped node and a second source-drain terminal coupled to the output terminal; and

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal responsive to a transition of the output enable signal to a magnitude sufficient to allow a pumped voltage generated at the pumped node to be coupled through the transistor to the output terminal.

7. The charge pump of claim 1 wherein the control circuit comprises:

an oscillator generating a periodic signal; and

a logic circuit coupled to receive the periodic signal from the oscillator, the logic circuit being operable to generate the charge enable signal, the first and second control signals, the first isolation signal, and the output enable signal in a timed sequence based on the periodic signal.

8. The charge pump of claim 1 wherein the first and second capacitors each comprise a transistor having its drain and source terminals coupled to each other to form one of the first and second terminals and its gate forming the other of the first and second terminals.

9. A charge pump, comprising:

a first capacitor having first and second terminals, the first terminal being coupled to a pumped node;

a second capacitor having first and second terminals, the first terminal being coupled to the pumped node;

a charging circuit coupled to the pumped node, the charging circuit being operable to charge the first and second capacitors through the pumped node during a charging period;

a first pumping circuit coupled to the second terminal of the first capacitor, the first pumping circuit being operable to increase the voltage at the second terminal of the first capacitor during a first pumping period following the charging period;

an isolation circuit operable to isolate the second terminal of the first capacitor during an isolation period following the first pumping period;

a second pumping circuit coupled to the second terminal of the second capacitor, the second pumping circuit being operable to increase the voltage at the second terminal of the second capacitor during a second pumping period that encompasses the isolation period; and

an output circuit coupled to the pumped node, the output circuit being operable to couple the pumped node to an output terminal during an output period that that encompasses the isolation period and the second pumping period.

10. The charge pump of claim 9 wherein the first isolation circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to the second terminal of the first capacitor and a second source-drain terminal coupled to receive the output signal of the first pumping circuit;

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal before the isolation period to a magnitude sufficient to allow the transistor to pass the increased voltage applied to the second terminal of the first capacitor.

11. The charge pump of claim 9 wherein the charging circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to a charging voltage and a second source-drain terminal coupled to the pumped node; and

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal during the charging period to a magnitude sufficient to allow a charging voltage to be coupled through the transistor to the pumped node.

12. The charge pump of claim 9 wherein the output circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to the pumped node and a second source-drain terminal coupled to the output terminal; and

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal during the output period to a magnitude sufficient to allow a pumped voltage generated at the pumped node to be coupled through the transistor to the output terminal.

13. The charge pump of claim 9 wherein the first and second capacitors each comprise a transistor having its drain and source terminals coupled to each other to form one of the first and second terminals and its gate forming the other of the first and second terminals.

14. A memory device, comprising:

a row address circuit operable to receive row address signals applied to an external terminal and to decode the row address signals to provide a row address;

a column address circuit operable to receive column address signals applied to an external terminal and to decode the column address signals to provide a column address;

at least one array of memory cells operable to store data written to or read from the array at a location determined by the row address and the column address;

a data path circuit operable to couple data signals corresponding to the data between the at least one array and an external data terminal;

a command signal generator operable to generate a sequence of control signals corresponding to command signals applied to an external terminal; and

a charge pump coupled to supply power to at least one component in the memory device, the charge pump comprising:

a first capacitor having first and second terminals, the first terminal being coupled to a pumped node;

a second capacitor having first and second terminals, the first terminal being coupled to the pumped node;

a charging circuit coupled to the pumped node, the charging circuit being operable to charge the first and second capacitors through the pumped node responsive to a charge enable signal;

a first pumping circuit having an output signal, the first pumping circuit transitioning the output signal from a first logic level to a second logic level responsive to a predetermined transition of a first control signal;

a second pumping circuit having an output signal, the second pumping circuit transitioning the output signal from a third logic level to a fourth logic level responsive to a predetermined transition of a second control signal;

a first isolation circuit coupled between the output of the first pumping circuit and the second terminal of the first capacitor, the first isolation circuit isolating the first pumping circuit from the second terminal of the first capacitor responsive to a first logic level of an isolation signal and coupling the output of the first pumping circuit to the second terminal of the first capacitor responsive to a second logic level of the isolation signal; and

an output circuit coupled to the pumped node, the output circuit being operable to couple the pumped node to the at least one component in the memory device responsive to an output enable signal; and

a control circuit operable to generate the charge enable signal, the first and second control signals, the first isolation signal, and the output enable signal.

15. The memory device of claim 14, wherein the control circuit is operable to generate the charge enable signal, the first, second, third and fourth control signals, the first and second isolation signals, and the output enable signal in the order of:

the charge enable signal;

the predetermined transition of the first control signal;

the first isolation signal;

the predetermined transition of the second control signal; and

the output enable signal.

16. The memory device of claim 14, further comprising:

a second isolation circuit coupled between the output of the second pumping circuit and the second terminal of the second capacitor, the second isolation circuit isolating the second pumping circuit from the second terminal of the second capacitor responsive to a first logic level of a second isolation signal and coupling the output of the second pumping circuit to the second terminal of the second capacitor responsive to a second logic level of the second isolation signal; and

wherein the control circuit is further operable to generate the second isolation signal.

17. The memory device of claim 14 wherein the first isolation circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to the second terminal of the first capacitor and a second source-drain terminal coupled to receive the output signal of the first pumping circuit;

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal responsive to a transition of the isolation signal from the first logic level to the second logic level to a magnitude sufficient to allow the transistor to pass the second logic level of the output from the first pumping circuit to the second terminal of the first capacitor.

18. The memory device of claim 14 wherein the charging circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to a charging voltage and a second source-drain terminal coupled to the pumped node; and

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal responsive to a transition of the charge enable signal to a magnitude sufficient to allow the charging voltage to be coupled through the transistor to the pumped node.

19. The memory device of claim 14 wherein the output circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to the pumped node and a second source-drain terminal coupled to the output terminal; and

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal responsive to a transition of the output enable signal to a magnitude sufficient to allow a pumped voltage generated at the pumped node to be coupled through the transistor to the output terminal.

20. The memory device of claim 14 wherein the control circuit comprises:

an oscillator generating a periodic signal; and

a logic circuit coupled to receive the periodic signal from the oscillator, the logic circuit being operable to generate the charge enable signal, the first and second control signals, the first isolation signal, and the output enable signal in a timed sequence based on the periodic signal.

21. The memory device of claim 14 wherein the row address circuit comprises a word line driver operable to generate row activate signals for coupling to word lines in the at least one array of memory cells, and wherein the at least one component in the memory device to which the pumped node is coupled comprises the word line driver.

22. The memory device of claim 14 wherein the at least one array of memory cells is fabricated in a semiconductor substrate, and wherein the at least one

component in the memory device to which the pumped node is coupled comprises the semiconductor substrate within which the at least one array of memory cells is fabricated.

23. The memory device of claim 14 wherein the data path circuit comprises a data output register operable to couple data signals to the external data terminal, and wherein the at least one component in the memory device to which the pumped node is coupled comprises the data output register.

24. A memory device, comprising:

a row address circuit operable to receive row address signals applied to an external terminal and to decode the row address signals to provide a row address;

a column address circuit operable to receive column address signals applied to an external terminal and to decode the column address signals to provide a column address;

at least one array of memory cells operable to store data written to or read from the array at a location determined by the row address and the column address;

a data path circuit operable to couple data signals corresponding to the data between the at least one array and an external data terminal;

a command signal generator operable to generate a sequence of control signals corresponding to command signals applied to an external terminal; and

a charge pump coupled to supply power to at least one component in the memory device, the charge pump comprising:

a first capacitor having first and second terminals, the first terminal being coupled to a pumped node;

a second capacitor having first and second terminals, the first terminal being coupled to the pumped node;

a charging circuit coupled to the pumped node, the charging circuit being operable to charge the first and second capacitors through the pumped node during a charging period;

a first pumping circuit coupled to the second terminal of the first capacitor, the first pumping circuit being operable to increase the voltage at the second

terminal of the first capacitor during a first pumping period following the charging period;

an isolation circuit operable to isolate the second terminal of the first capacitor during an isolation period following the first pumping period;

a second pumping circuit coupled to the second terminal of the second capacitor, the second pumping circuit being operable to increase the voltage at the second terminal of the second capacitor during a second pumping period that encompasses the isolation period; and

an output circuit coupled to the pumped node, the output circuit being operable to couple the pumped node to the at least one component in the memory device during an output period that that encompasses the isolation period and the second pumping period.

25. The memory device of claim 24 wherein the first isolation circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to the second terminal of the first capacitor and a second source-drain terminal coupled to receive the output signal of the first pumping circuit;

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal before the isolation period to a magnitude sufficient to allow the transistor to pass the increased voltage applied to the second terminal of the first capacitor.

26. The memory device of claim 24 wherein the charging circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to a charging voltage and a second source-drain terminal coupled to the pumped node; and

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal during the charging period to a

magnitude sufficient to allow a charging voltage to be coupled through the transistor to the pumped node.

27. The memory device of claim 24 wherein the output circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to the pumped node and a second source-drain terminal coupled to the output terminal; and

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal during the output period to a magnitude sufficient to allow a pumped voltage generated at the pumped node to be coupled through the transistor to the output terminal.

28. The memory device of claim 24 wherein the row address circuit comprises a word line driver operable to generate row activate signals for coupling to word lines in the at least one array of memory cells, and wherein the at least one component in the memory device to which the pumped node is coupled comprises the word line driver.

29. The memory device of claim 24 wherein the at least one array of memory cells is fabricated in a semiconductor substrate, and wherein the at least one component in the memory device to which the pumped node is coupled comprises the semiconductor substrate within which the at least one array of memory cells is fabricated.

30. The memory device of claim 24 wherein the data path circuit comprises a data output register operable to couple data signals to the external data terminal, and wherein the at least one component in the memory device to which the pumped node is coupled comprises the data output register.

31. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a memory device coupled to the processor bus adapted to allow data to be stored, the memory device comprising:

a row address circuit operable to receive row address signals applied to an external terminal and to decode the row address signals to provide a row address;

a column address circuit operable to receive column address signals applied to an external terminal and to decode the column address signals to provide a column address;

at least one array of memory cells operable to store data written to or read from the array at a location determined by the row address and the column address;

a data path circuit operable to couple data signals corresponding to the data between the at least one array and an external data terminal;

a command signal generator operable to generate a sequence of control signals corresponding to command signals applied to an external terminal; and

a charge pump coupled to supply power to at least one component in the memory device, the charge pump comprising:

a first capacitor having first and second terminals, the first terminal being coupled to a pumped node;

a second capacitor having first and second terminals, the first terminal being coupled to the pumped node;

a charging circuit coupled to the pumped node, the charging circuit being operable to charge the first and second capacitors through the pumped node responsive to a charge enable signal;

a first pumping circuit having an output signal, the first pumping circuit transitioning the output signal from a first logic level to a second logic level responsive to a predetermined transition of a first control signal;

a second pumping circuit having an output signal, the second pumping circuit transitioning the output signal from a third logic level to a fourth logic level responsive to a predetermined transition of a second control signal;

a first isolation circuit coupled between the output of the first pumping circuit and the second terminal of the first capacitor, the first isolation circuit isolating the first pumping circuit from the second terminal of the first capacitor responsive to a first logic level of an isolation signal and coupling the output of the first pumping circuit to the second terminal of the first capacitor responsive to a second logic level of the isolation signal; and

an output circuit coupled to the pumped node, the output circuit being operable to couple the pumped node to the at least one component in the memory device responsive to an output enable signal; and

a control circuit operable to generate the charge enable signal, the first and second control signals, the first isolation signal, and the output enable signal.

32. The computer system of claim 31, wherein the control circuit is operable to generate the charge enable signal, the first, second, third and fourth control signals, the first and second isolation signals, and the output enable signal in the order of:

the charge enable signal;

the predetermined transition of the first control signal;

the first isolation signal;

the predetermined transition of the second control signal; and

the output enable signal.

33. The computer system of claim 31, further comprising:

a second isolation circuit coupled between the output of the second pumping circuit and the second terminal of the second capacitor, the second isolation circuit isolating the second pumping circuit from the second terminal of the second capacitor responsive to a first logic level of a second isolation signal and coupling the output of the second pumping

circuit to the second terminal of the second capacitor responsive to a second logic level of the second isolation signal; and

wherein the control circuit is further operable to generate the second isolation signal.

34. The computer system of claim 31 wherein the first isolation circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to the second terminal of the first capacitor and a second source-drain terminal coupled to receive the output signal of the first pumping circuit;

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal responsive to a transition of the isolation signal from the first logic level to the second logic level to a magnitude sufficient to allow the transistor to pass the second logic level of the output from the first pumping circuit to the second terminal of the first capacitor.

35. The computer system of claim 31 wherein the charging circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to a charging voltage and a second source-drain terminal coupled to the pumped node; and

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal responsive to a transition of the charge enable signal to a magnitude sufficient to allow the charging voltage to be coupled through the transistor to the pumped node.

36. The computer system of claim 31 wherein the output circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to the pumped node and a second source-drain terminal coupled to the output terminal; and

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal responsive to a transition of the output

enable signal to a magnitude sufficient to allow a pumped voltage generated at the pumped node to be coupled through the transistor to the output terminal.

37. The computer system of claim 31 wherein the control circuit comprises:

an oscillator generating a periodic signal; and

a logic circuit coupled to receive the periodic signal from the oscillator, the logic circuit being operable to generate the charge enable signal, the first and second control signals, the first isolation signal, and the output enable signal in a timed sequence based on the periodic signal.

38. The computer system of claim 31 wherein the row address circuit comprises a word line driver operable to generate row activate signals for coupling to word lines in the at least one array of memory cells, and wherein the at least one component in the memory device to which the pumped node is coupled comprises the word line driver.

39. The computer system of claim 31 wherein the at least one array of memory cells is fabricated in a semiconductor substrate, and wherein the at least one component in the memory device to which the pumped node is coupled comprises the semiconductor substrate within which the at least one array of memory cells is fabricated.

40. The computer system of claim 31 wherein the data path circuit comprises a data output register operable to couple data signals to the external data terminal, and wherein the at least one component in the memory device to which the pumped node is coupled comprises the data output register.

41. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a memory device coupled to the processor bus adapted to allow data to be stored, the memory device comprising:

a row address circuit operable to receive row address signals applied to an external terminal and to decode the row address signals to provide a row address;

a column address circuit operable to receive column address signals applied to an external terminal and to decode the column address signals to provide a column address;

at least one array of memory cells operable to store data written to or read from the array at a location determined by the row address and the column address;

a data path circuit operable to couple data signals corresponding to the data between the at least one array and an external data terminal;

a command signal generator operable to generate a sequence of control signals corresponding to command signals applied to an external terminal; and

a charge pump coupled to supply power to at least one component in the memory device, the charge pump comprising:

a first capacitor having first and second terminals, the first terminal being coupled to a pumped node;

a second capacitor having first and second terminals, the first terminal being coupled to the pumped node;

a charging circuit coupled to the pumped node, the charging circuit being operable to charge the first and second capacitors through the pumped node during a charging period;

a first pumping circuit coupled to the second terminal of the first capacitor, the first pumping circuit being operable to increase the voltage at the second terminal of the first capacitor during a first pumping period following the charging period;

an isolation circuit operable to isolate the second terminal of the first capacitor during an isolation period following the first pumping period;

a second pumping circuit coupled to the second terminal of the second capacitor, the second pumping circuit being operable to increase the voltage at the second terminal of the second capacitor during a second pumping period that encompasses the isolation period; and

an output circuit coupled to the pumped node, the output circuit being operable to couple the pumped node to the at least one component in the memory device during an output period that that encompasses the isolation period and the second pumping period.

42. The computer system of claim 41 wherein the first isolation circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to the second terminal of the first capacitor and a second source-drain terminal coupled to receive the output signal of the first pumping circuit;

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal before the isolation period to a magnitude sufficient to allow the transistor to pass the increased voltage applied to the second terminal of the first capacitor.

43. The computer system of claim 41 wherein the charging circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to a charging voltage and a second source-drain terminal coupled to the pumped node; and

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal during the charging period to a magnitude sufficient to allow a charging voltage to be coupled through the transistor to the pumped node.

44. The computer system of claim 41 wherein the output circuit comprises:

a transistor having a gate terminal, a first source-drain terminal coupled to the pumped node and a second source-drain terminal coupled to the output terminal; and

a charge pump circuit coupled to the gate terminal of the transistor, the charge pump circuit increasing the voltage at the gate terminal during the output period to a magnitude sufficient to allow a pumped voltage generated at the pumped node to be coupled through the transistor to the output terminal.

45. The computer system of claim 41 wherein the row address circuit comprises a word line driver operable to generate row activate signals for coupling to word lines in the at least one array of memory cells, and wherein the at least one component in the memory device to which the pumped node is coupled comprises the word line driver.

46. The computer system of claim 41 wherein the at least one array of memory cells is fabricated in a semiconductor substrate, and wherein the at least one component in the memory device to which the pumped node is coupled comprises the semiconductor substrate within which the at least one array of memory cells is fabricated.

47. The computer system of claim 41 wherein the data path circuit comprises a data output register operable to couple data signals to the external data terminal, and wherein the at least one component in the memory device to which the pumped node is coupled comprises the data output register.

48. A method of generating a pumped voltage having a magnitude that is substantially greater than the magnitude of a supply voltage, comprising:

coupling a first terminal of each of a plurality of capacitors to a pumped node;

while a second terminal of each of the capacitors is at a first voltage, charging the capacitors;

sequentially changing the voltage at the second terminal of each of the capacitors from the first voltage to a second voltage; and

except for a final one of the capacitors, after changing the voltage at the second terminal of each of the capacitors from the first voltage to a second voltage but before subsequently changing the voltage at the second terminal of one of the capacitors from the first voltage to the second voltage, isolating the second terminal of the capacitor.

49. The method of claim 48 wherein the act of coupling a first terminal of each of a plurality of capacitors to a pumped node comprises coupling a first terminal of two capacitors to a pumped node.

50. The method of claim 48, further comprising selectively coupling the pumped node to an output terminal.

51. The method of claim 48 wherein the act of charging the capacitors while the second terminal of each of the capacitors is at the first voltage comprises charging the capacitors to substantially the supply voltage while the second terminal of each of the capacitors is at ground potential, and wherein the act of changing the voltage at the second terminal of each of the capacitors from the first voltage to the second voltage comprises changing the voltage at the second terminal of each of the capacitors from ground potential to substantially the supply voltage.

52. A method of generating a pumped voltage, comprising:

coupling a first terminal of each of a plurality of capacitors to a pumped node;

sequentially pumping a second terminal of each of the plurality of capacitors; and

sharing the charge of each of the capacitors being pumped with N other capacitors, the number N decreasing by one as each of the capacitors is pumped.

53. The method of claim 52 wherein the act of sharing the charge of each of the capacitors being pumped with N other capacitors, the number N decreasing by one as

each of the capacitors is pumped comprises, after pumping a plurality of the capacitors, isolating the second terminal of the capacitor that has been pumped.